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Development of the Photomultiplier-Tube Readout System for the CTA Large Size Telescope

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Abstract: We have developed a prototype of the photomultiplier tube (PMT) readout system for the Cherenkov Telescope Array (CTA) Large Size Telescope (LST). Two thousand PMTs along with their readout systems are arranged on the focal plane of each telescope, with one readout system per 7-PMT cluster. The Cherenkov light pulses generated by the air showers are detected by the PMTs and amplified in a compact, low noise and wide dynamic range gain block. The output of this block is then digitized at a sampling rate of the order of GHz using the Domino Ring Sampler DRS4, an analog memory ASIC developed at Paul Scherrer Institute. The sampler has 1,024 capacitors per channel and four channels are cascaded for increased depth. After a trigger is generated in the system, the charges stored in the capacitors are digitized by an external slow sampling ADC and then transmitted via Gigabit Ethernet. An onboard FPGA controls the DRS4, trigger threshold, and Ethernet transfer. In addition, the control and monitoring of the Cockcroft-Walton circuit that provides high voltage for the 7-PMT cluster are performed by the same FPGA. A prototype named *Dragon* has been developed that has successfully sampled PMT signals at a rate of 2 GHz, and generated single photoelectron spectra.

Keywords: Imaging Atmospheric Cherenkov Telescope, Gamma-rays, Electronics

1 Introduction

A ground-based imaging atmospheric Cherenkov telescope (IACT) measures Cherenkov light from an extended air shower (EAS) generated by the interaction between very high energy (VHE) gamma rays and the upper atmosphere. Night sky background (NSB) also enters a pixel photon sensor of the focal plane of the IACT with a rate of the order of 10–100 MHz, depending on the mirror size and the pixel size. In some region of the Galactic plane, the NSB can reach on average up to several hundred MHz. The NSB therefore becomes noise that affects the sensitivity and the energy threshold. Given this NSB pollution, and the fact that the duration of Cherenkov light from EAS is a few nanoseconds, a fast digitization speed of the readout system coupled to a fast photosensor like a photomultiplier tube (PMT) is beneficial to increase the pixels' signal-

to-noise ratio. In addition, this system should be compact and have low cost and low power consumption because each IACT possesses several thousand photon sensor pixels and the readout system attached to the sensors is in a camera container located at the focal position. Furthermore, a wide dynamic range of more than 8–10 bits is required to resolve a single photoelectron and have a wider energy range.

A commercial flash analog-to-digital converter (FADC) satisfies the requirement of a wide dynamic range. However, it is costly and consumes relatively high power of a few watts per channel. On the other hand, an analog memory application specific integrated circuit (ASIC), that consists of several hundred to several thousand switched capacitor arrays (SCA) per channel, can sample a signal at the order of GHz, with a wide dynamic range and lower power consumption. Several types of analog memory ASICs have been developed for applications in particle physics and cosmic ray physics. With respect to IACTs, a modified version of ARS0 [1], Swift Analog Memory (SAM) [2], and Domino Ring Sampler (DRS) [3] chips are used in the H.E.S.S.-I, H.E.S.S.-II, and MAGIC experiments, respectively.

Cherenkov Telescope Array (CTA) [4] is the next generation VHE gamma-ray observatory, which improves the sensitivity by a factor of 10 in the range 100 GeV–10 TeV and an extension to energies well below 100 GeV and above 100 TeV. CTA consists of telescopes having mirrors with size 23 m, 12 m, 3.5–7 m, and $\sim$50 m^2, which are called large size telescope (LST), medium size telescope (MST), small size telescope (SST), and Schwarzschild-Couder telescope (SCT), respectively. Several types of readout systems are developed for CTA with different analog memories for the requirements of LST, MST, SST, and SCT. At the same time, there has been progress in the development of photon sensors such as PMT and a Geiger-mode avalanche photodiode (or silicon photomultiplier) for CTA. At this time, the primary candidate for LST is a PMT.

Using the analog memory DRS version 4 (hereafter DRS4), we have so far developed three versions of prototypes for the PMT readout system for CTA, named *Dragon*. Using the first version of the prototype, we demonstrated that the waveform of a PMT signal can be well digitized with the DRS4 chip. The second version was developed with improvements made to the sampling depth of DRS4 and a trigger [5]. The third version was developed to be downsized and reduce the cost for mass production. In this paper, we report the design and performance of the third version of the prototype.

2 Design of Readout System

2.1 Overview

Two thousand PMTs and their readout systems are arranged on the focal plane of each LST telescope [6], with one readout system per 7-PMT cluster. We have developed the third prototype of the PMT readout system. Figures 1 and 2 show a photograph and block diagram of the prototype, respectively. The prototype consists of a 7-PMT cluster, a slow control board and a DRS4 readout board. The total size is 14 cm $\times$ 48 cm. The 7-PMT cluster and the slow control board are described in detail in reference [7]. In this paper, a brief description is provided.

Our 7-PMT cluster consists of seven head-on type PMTs with a super-bialkali photocathode and 8-stage dynodes (Hamamatsu Photonics, R11920-100 with a diameter of 38 mm) [8], a Cockcroft-Walton (CW) circuit for high voltage supply to the PMTs (designed by Hamamatsu Photonics), and a preamplifier board. A signal from the PMT is amplified by a preamplifier, and fed to the DRS4 readout board. A commercial preamplifier, Mini-circuits LEE-39+, is used in the current *Dragon* (Fig. 3). A preamplifier board with an ASIC designed for CTA, PACTA [9], has been recently developed and will be used in the next *Dragon*.

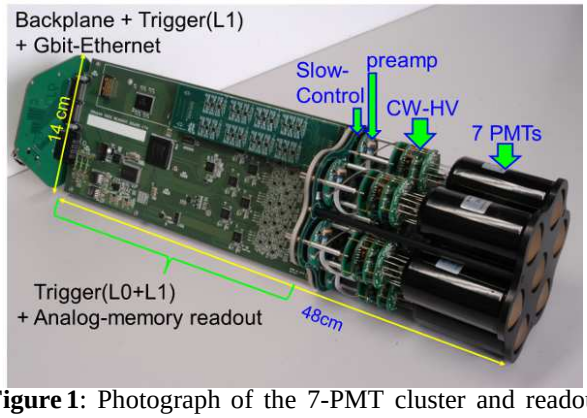

Figure 1: Photograph of the 7-PMT cluster and readout system (ver. 3).

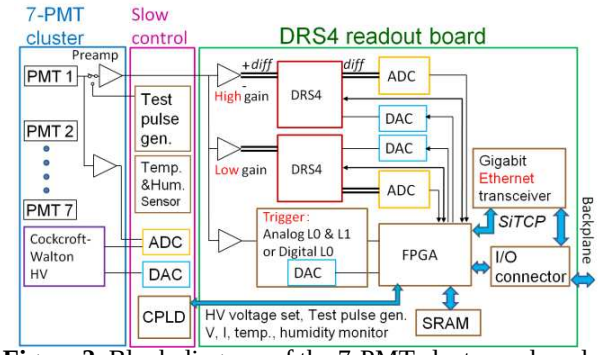

Figure 2: Block diagram of the 7-PMT cluster and readout system (ver. 3).

On the DRS4 readout board the preamplified signal is divided into three lines: a high gain channel, a low gain channel, and a trigger channel. The high and low gain channels are connected to DRS4 chips. The signal is sampled at a rate of the order of GHz and the waveform is stored in a SCA in DRS4. When a trigger is generated in the trigger circuit, the voltages stored in the capacitor array are sequentially output and then digitized by an external slow sampling ($\sim$30 MHz) ADC. The digitized data is sent to a field programmable gate array (FPGA) and then transmitted to a Gigabit Ethernet transceiver and a backplane via a data input/output (I/O) connector. The FPGA controls a static random access memory (SRAM) that stores large amounts of data before transmission and a digital-to-analog converter (DAC) used for thresholding in the trigger circuit.

The slow control board (Fig.1) is equipped with a generator for test pulses that are fed to the preamplifier, a temperature and humidity sensor with I2C interface, a DAC for setting the voltage of the CW high voltage circuit, and an ADC for monitoring both the CW circuit and the DC anode current. These devices on the slow control board are controlled by a complex programmable logic device

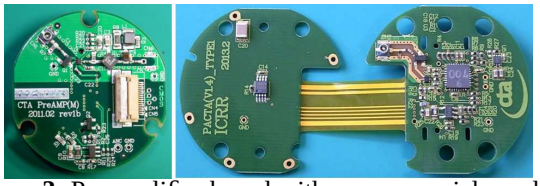

Figure 3: Preamplifier board with a commercial amplifier (left) and the PACTA (right).

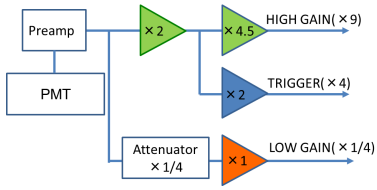

Figure 5: Block diagram of the main amplifiers.

(CPLD). Since the CPLD communicates with the FPGA on the DRS4 readout board, the data to and from the CPLD is sent via the Ethernet. The power supply to the DRS4 readout board and the slow control board is ±3.3V and +5V. The total power consumption is ∼2W per readout channel.

2.2 DRS4 Readout Board

Figure 4 shows a photograph of the DRS4 readout board with a size of 14 cm × 30 cm, 10 cm shorter than the version 2. The slow control board attached to the 7-PMT cluster is connected to the DRS4 readout board from the right side via two card-edge connectors. The DRS4 board has main amplifiers, eight DRS4 chips, ADCs for digitizing a signal stored in the capacitor array in DRS4 at a sampling frequency of 33 MHz, a DAC to control the DRS4, an FPGA, a 18Mbit SRAM, a Gigabit Ethernet transceiver, and a data I/O connector to the backplane. A Xilinx Vertex-4 FPGA was adopted in the version 2. In the version 3, a Xilinx Spartan-6 FPGA is used to reduce the cost for mass production. In addition, analog level 0 (L0) and 1 (L1) trigger mezzanines or a digital level 0 (L0) trigger mezzanine are mounted on the DRS4 board. Details of these parts are described in the following subsections.

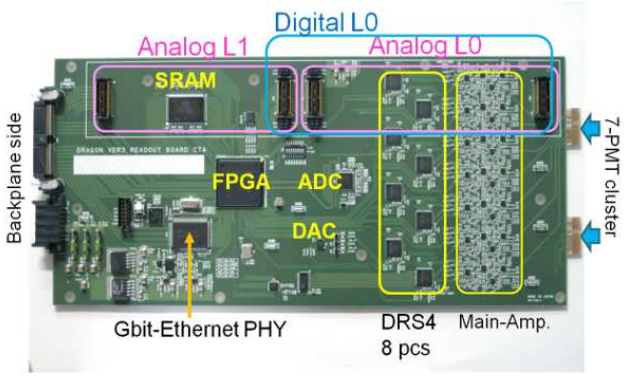

Figure 4: Photograph of the DRS4 readout board (ver. 3).

2.3 Main Amplifier

Figure 5 shows a block diagram of the main amplifiers. It is designed to have a bandwidth greater than 250 MHz for the high gain channel, lower power consumption, and a dynamic range of 0.2-1000 photoelectrons for LST. A preamplified signal from a PMT with a typical gain of 4 × 10^4 is fed to the main amplifier. The signal is amplified using two differential amplifiers to meet the requirement for bandwidth and power consumption. For the high gain channel, it is amplified by a gain of 9 using Analog Devices, ADA4927. For the trigger, it is amplified by a gain of 4 using Analog Devices, ADA4927 and ADA4950. For the low gain channel, the preamplified signal is attenuated by 1/4 and then buffered with a differential amplifier using Analog Devices, ADA4950.

2.4 Trigger

The DRS4 readout board has been designed to host an analog trigger [10] or digital trigger [5]. The different elements of the trigger system will be placed at different locations on the readout electronics, as shown in Fig. 4.

For the analog trigger, the decision boards (L0/L1) are placed on the readout board itself, while for the digital trigger the L0 board is placed in the frontend and the L1 in the backplane, keeping both analog and digital L0 as close as possible after the signals from PMTs. The distribution boards are placed at the backplane of the readout board, in order to send and receive trigger signals efficiently among neighbouring clusters. The choice of using trigger mezzanines and sharing of connectors has allowed the independent study of both analog and digital solution in the development phase.

2.5 DRS4 Chip

The DRS chip is being developed at the Paul Scherrer Institute (PSI), Switzerland, for the MEG experiment [3]. The latest version, DRS4, is also used in the MAGIC experiment. The DRS4 chip includes nine differential input channels at a sampling speed of 700 MS/s–5 GS/s, with a bandwidth of 950 MHz, and a low noise of 0.35 mV after offset correction. The analog waveform is stored in 1,024 sampling capacitors per channel and the waveform can be read out after sampling via a shift register that is clocked at a maximum of 33 MHz for digitization using an external ADC. The power consumption of the DRS4 chip is 17.5 mW per channel at 2 GS/s sampling rate. The chip is fabricated using the 0.25 μm CMOS technology.

It is possible to cascade two or more channels to obtain deeper sampling depth. In the *Dragon*, four channels were cascaded, leading to a sampling depth of 4,096 for each PMT signal, which corresponds to a depth of 4 μs at 1 GS/s sampling rate. It enables continuous sampling until the stereo coincidence trigger confirms the local telescope trigger, and initializes the camera readout.

2.6 FPGA-based Gigabit Ethernet (SiTCP)

The digitized waveform data and the monitor/control data are transmitted via Ethernet with only two devices: FPGA and Gigabit Ethernet transceiver (PHY). This simple composition is available on a hardware-based TCP processor, SiTCP [11]. The circuit size of SiTCP in the FPGA is ∼3000 slices, which is small enough to allow implementation with user circuits on a single FPGA. In addition, the SiTCP has an advantage in that the throughputs in both directions can simultaneously reach the theoretical upper limits of Gigabit Ethernet.

2.7 Mini-Camera with Three Clusters

A prototype with three clusters of PMTs and their readout boards was constructed to develop the trigger system between multiple clusters (Fig. 6) [10].

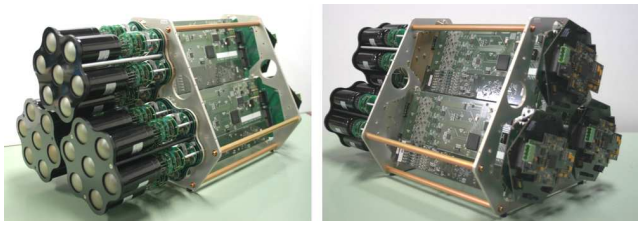

Figure 6: Prototype with three clusters of PMTs and their readout boards.

3 Performance of Readout System

The performance of the DRS4 readout system *Dragon* was measured. Figure 7 shows that dynamic ranges of high and low gain channels are 60 p.e. and 2500 p.e., which satisfied the requirement of $>$1000 photoelectrons. Measured noise level for the high gain channel is 0.1 p.e. (rms).

Figure 8 shows normalized gains for high and low gain channels as a function of frequency. The bandwidths for high and low gain channels are 260 MHz and 190 MHz at -3dB, respectively while those of the DRS4 readout board combined with a preamplifier (LEE-39+) were 250 MHz and 180 MHz at -3dB for high and low gain channels, respectively.

After the above measurements, the performance of the DRS4 readout board attached to a PMT was investigated. Figure 9 shows a pulse shape of the high gain channel of the PMT signal with a gain of 5×10^4, which was measured with a UV laser and the DRS4 readout system at a sampling rate of 2 GS/s. The PMT signal having a width of $\sim$3 ns (FWHM) and a height corresponding to $\sim$3 photoelectrons was successfully digitized. Measured dead time for readout of 60 cells in the DRS4 chip is 0.9% and 5.4% at 1 kHz and 7 kHz, respectively. Figure 10 shows a single photoelectron spectrum of the high gain channel of the PMT signal with a gain of 5×10^4, which was measured with *Dragon* and an LED at a sampling rate of 2 GS/s. In the figure, a single photoelectron peak is clearly seen. The signal to noise ratio defined as (single-photoelectron mean - pedestal mean) / pedestal r.m.s. is 3.6.

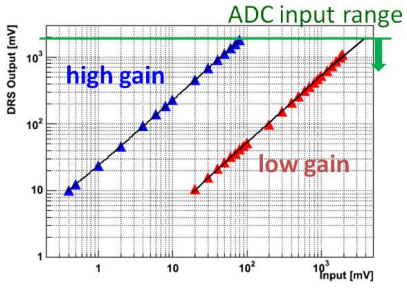

Figure 7: Dynamic ranges of the DRS4 readout board.

4 Conclusion

We have developed a prototype 7-PMT cluster readout system for the large-size telescope of the next generation VHE gamma ray observatory, CTA. In the readout system named *Dragon*, a PMT signal is amplified, and its waveform is then digitized at a sampling rate of the order of GHz using an analog memory ASIC DRS4 that has 4,096 capacitors per readout channel. Using the prototype system attached to a PMT with a Cockcroft-Walton circuit, we successfully obtained a pulse shape of the signal of the PMT detecting a UV light at a sampling rate of 2 GS/s, and also a single photoelectron spectrum. Evaluation of the readout system's performance is ongoing, and a prototype with several dozen clusters and their readout boards will be constructed as the next step for the development of a full telescope camera.

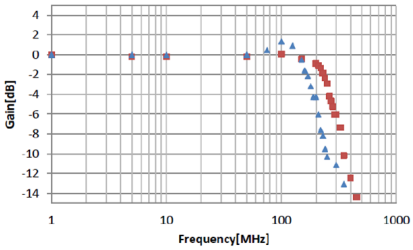

Figure 8: Bandwidths of high-(square) and low-(triangle) gain channels.

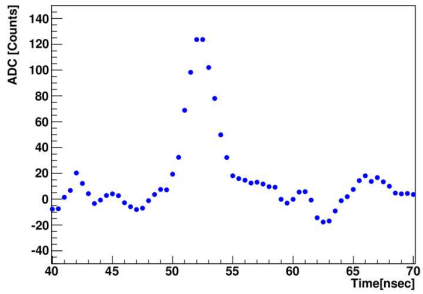

Figure 9: Pulse shape of the PMT signal measured with the DRS4 readout system at a sampling rate of 2 GS/s.

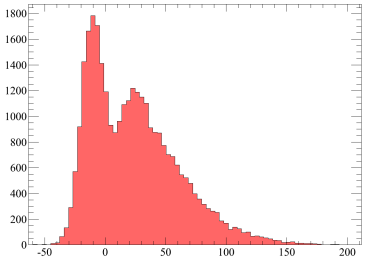

Figure 10: Single photoelectron spectrum of the PMT signal measured with the DRS4 readout system. The horizontal axis is in units of mV $\times$ ns.

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